What is claimed is:

1. A semiconductor integrated circuit device comprising:

a first MOS transistor

having a first backgate region, a first conductive region, and a second conductive region, and

having the first backgate region and the first conductive region thereof connected together;

a second MOS transistor

having a second backgate region, a third conductive region, and a fourth conductive region,

having the second backgate region and the third conductive region thereof connected to the first backgate region and the first conductive region of the first MOS transistor, and

receiving at the fourth conductive region thereof a first direct-current voltage;

a voltage setting circuit

setting a second direct-current voltage fed to a gate of the second MOS transistor; and

an anti-reverse-current element

receiving the first direct-current voltage or a third direct-current voltage produced from the first direct-current voltage, and

connected to the voltage setting circuit in such a way as to prevent a reverse current from flowing through the voltage setting circuit,

wherein the voltage setting circuit produces, according to the first direct-

current voltage or the third direct-current voltage, the second direct-current voltage within a withstand voltage range of the second MOS transistor.

2. A semiconductor integrated circuit device as clamed in claim 1, wherein the first and second MOS transistors are of a same polarity.

3. A semiconductor integrated circuit device as clamed in claim 1, wherein the anti-reverse-current element is a diode.

4. A semiconductor integrated circuit device as clamed in claim 1, wherein the voltage setting circuit is composed of voltage-division resistors.

5. A semiconductor integrated circuit device comprising:

a first MOS transistor of a P-channel type

having a backgate and a first P-type diffusion layer thereof connected together;

a second MOS transistor of a P-channel type

having a backgate and a third P-type diffusion layer thereof connected to the backgate and the first P-type diffusion layer of the first MOS transistor, and

receiving at a fourth P-type diffusion layer thereof a first direct-current voltage;

a voltage-division resistor circuit

having one end thereof grounded, and

feeding, as a second direct-current voltage, a division voltage

produced thereby to a gate of the second MOS transistor; and

a diode

receiving at an anode thereof the first direct-current voltage or a third direct-current voltage produced from the first direct-current voltage, and

having a cathode thereof connected to another end of the voltage-division resistor circuit,

wherein the second direct-current voltage from the voltage-division resistor circuit is kept within a withstand voltage range of the second MOS transistor according to the first direct-current voltage or the third direct-current voltage.